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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,667	07/29/2003	Timothy E. Fiscus	0325.00519c	6489

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EXAMINER	
MAI, SON LUU	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,667	FISCUS ET AL.	
	Examiner	Art Unit	
	Son L. Mai	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27,28 and 31* is/are allowed.

6)☒ Claim(s) *1-26,29 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10-21-04 has been entered. Accordingly, claims 1-31 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-26, 29-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The currently amended claims 1, 10 and 11 have added the limitation " said background operations can be enabled simultaneously in each two or more of sections independently of any other section" which has no support from the originally filed specification. The specification only depicts a capability to refresh one-fourth, one-half, three-quarters and/or all of the memory array space of a

DRAM. Claims 2-9, 12-26, 29 and 30 are rejected for including the limitations of independent claims 1 and 11.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 5-8, 10-19, 21-26, 29-30, as best understood in view of 112, first paragraph rejection above, are rejected under 35 U.S.C. 102(b) as being anticipated by Arimoto (U.S. Patent 5,798,976).

Regarding claim 1, Arimoto discloses a method for reducing power consumption during background operations (refresh operations; see Abstract) in a memory array with a plurality of sections (4 sections MA#0-MA#3 as shown in figure 2) comprising the steps of: controlling said background operations in one or more of said plurality of sections of said memory array in response to one or more control signals (from array control circuit 12); wherein said background operations can be enabled in each of said plurality of sections independently of any other section (column 4, lines 50-53); and presenting said one or more control signals and one or more decoded address signals (from row address buffer 16) to one or more periphery array circuits (as shown in figure 33) of said one or more sections.

Regarding claim 2, Arimoto teaches the method according to claim 1 wherein said background operations comprise a refresh operation (see Abstract).

Regarding claim 3, Arimoto teaches the method according to claim 1, wherein said plurality of sections comprise quadrants (4 sections MA#0-MA#3 as shown in figure 2).

Regarding claim 5, Arimoto discloses the method according to claim 1, further comprising: controlling, in response to said one or more control signals, an operation of said one or more periphery array circuits, wherein said periphery array circuits each comprise one or more circuits from the group consisting of sense amplifiers (SENSE AMP in figure 33), column multiplexer circuits (not shown but understood), equalization circuits (84), and wordline driver circuits (85).

Regarding claim 6, Arimoto discloses the method according to claim 1 further comprising: generating one of said one or more control signals for each of said plurality of sections of said memory array (each section receives control signals as shown in figure 2.)

Regarding claim 7, Arimoto teaches the method according to claim 1, wherein said one or more control signals are generated in response to an address signal (signal RA in figure 2.)

Regarding claim 8, Arimoto teaches the method according to claim 1, further comprising: generating said one or more control signals in response to a refresh enable signal (signal ZRAS in figure 3.)

Regarding claim 10, Arimoto teaches an apparatus comprising: means for controlling a background operation (refresh operation) in one or more sections (4 MA#0-MA#3 as shown in figure 2) of a memory array in response to one or more control

signals (from array control circuit 12); wherein said background operations can be enabled in each of said plurality of sections independently of any other section (column 4, lines 50-53); and means for presenting said one or more control signals and one or more decoded address signals (signals RA) to one or more periphery array circuits (as shown in figure 33) of said one or more sections.

Regarding claim 11, Arimoto teaches an apparatus comprising: a memory array comprising a plurality of sections (4 sections MA#0-MA#3 as shown in figure 2), wherein each of said sections comprises (i) a plurality of memory cells (MC in figure 33) and (ii) periphery array circuitry (83, 85, 87,) configured to control access to said plurality of memory cells; and a control circuit (12, 16 in figure 2) configured to present one or more control signals and one or more decoded address signals to said periphery array circuitry of said plurality of sections, wherein a background operation (refresh operation) in each of said plurality of sections (i) is controlled in response to said one or more control signals and (ii) can be enabled independently of any other section (column 4, lines 50-53.)

Regarding claim 12, Arimoto discloses the apparatus according to claim 11, wherein said a refresh operation comprises background operation (see Abstract).

Regarding claim 13, Arimoto teaches the apparatus according to claim 11, wherein each of said one or more control signals is configured to control one or more array control signals of a corresponding section (figure 2 shows each section is controlled by control signals from circuits 12 and 16).

Regarding claim 14, Arimoto teaches the apparatus periphery according to claim 11, wherein said [periphery] array circuitry (83, 85, 87,) comprises one or more sense amplifiers (20 in figure 33) configured to sense a memory cell state in response to said one or more control signals (from circuits 83, 87...) and said one or more decoded address signals (from circuit 85).

Regarding claim 15, Arimoto teaches the apparatus according to claim 11, wherein said periphery array circuitry is configured to generate one or more wordline signals (WL in figure 9) in response to said one or more control signals (MS) and said one or more decoded address signals (RA).

Regarding claim 16, Arimoto teaches the apparatus according to claim 11, wherein said periphery array circuitry (83, 85, 87...) comprises equalization circuitry (84) configured to equalize one or more bitlines (BL) to a predetermined voltage potential in response to said one or more control signals (EQ) and said one or more decoded address signals (from circuit 85.)

Regarding claim 17, Arimoto teaches the apparatus according to claim wherein said periphery array circuitry comprises column multiplexing circuitry (not shown but understood as means to select a column for a refresh, read or write operation.)

Regarding claim 18, Arimoto teaches the apparatus according to claim 11, wherein said one or more control signals are generated in response to an address signal (RA in figure 2).

Regarding claim 19, Arimoto teaches the apparatus according to claim 11, wherein each of said memory cells comprises a dynamic storage element (MC in figure 33.)

Regarding claim 21, Arimoto teaches the apparatus according to claim 11, wherein said one or more decoded address signals comprise one or more decoded row address signals and one or more decoded column address signals (signals RA and BS in figure 26A.)

Regarding claim 22, Arimoto teaches the apparatus according to claim 11, wherein said periphery array circuitry of each of said plurality of sections is configured to control said plurality of memory cells of each of said plurality of sections response to said one or more control signals and said one or more decoded address signals (figure 2 shows each section is controlled by control signals from circuits 12 and 16).

Regarding claim 23, Arimoto teaches the apparatus according to claim 11, wherein said memory array comprises a plurality of blocks and each block of said plurality of blocks comprises two or more of said plurality of sections (a block comprises memory arrays MA#0 and MA#0).

Regarding claim 24, Arimoto teaches the method according to claim 1, wherein said one or more decoded address signals comprise one or more decoded row address signals and one or more decoded column address signals. (signals RA and BS in figure 26A.)

Regarding claim 25, Arimoto teaches the method according to claim 1, wherein said background operations (refresh operations) are enabled in response to a first state

of said one or more control signals. (figure 3 shows a refresh operation is enable when ext/RAS and ext/CAS are low)

Regarding claim 26, Arimoto teaches the method according to claim 1, wherein said background operations are disabled in response to a first state of said one or more control signals (figure 3 shows a refresh operation is disable when ext/RAS and ext/CAS are high).

Regarding claims 29 and 30, the address signal (RA) as taught by Arimoto is programmable as a result of a multiplexer (14 in figure 2) and signals from refresh control circuit.

Allowable Subject Matter

6. Claims 27, 28 and 31 are allowed.

7. The reasons for allowance were provided in the Office action mailed 03-11-04.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mizugaki (U.S. Patent 6560153) discloses refresh operations of memory sections in a DRAM during background operations for reducing power consumption.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12-23-04

Son L. Mai
Primary Examiner
Art Unit 2818